

Sub B2 Cont  
forming a sacrificial layer having a relatively planar top surface over the semiconductor substrate, the sacrificial layer comprising a portion covering the hard mask layer and a portion filling the gap; and

AX (Cmet.)  
removing the sacrificial layer and the hard mask layer with a single etch process, wherein an etch rate of the sacrificial layer and an etch rate of the hard mask layer are selected to substantially completely remove the portion of the sacrificial layer covering the hard mask and the hard mask layer, and wherein the etch rate of the hard mask layer is substantially greater than the silicon layer.

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A1 Cont.  
25. (New) The method of claim 24, wherein removing the sacrificial layer and the hard mask layer with a single etch process further comprises substantially completely removing the portion of the portion of the sacrificial layer filling the gap along with the portion of the sacrificial layer covering the hard mask and the hard mask layer.

26. (New) The method of claim 25, wherein the single etch process is a plasma etch process.

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